CLAIMS

1. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a first test pattern generation section, operating on a second clock having half the frequency of said first clock, for generating first test data,

a second test pattern generation section, operating on a third clock, the inverted clock of said second clock, for generating second test data, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on either the signal value of said second clock or the signal value of said third clock, thereby inputting the selected test data to said memory as third test data.

2. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a first test pattern generation section, operating on a second clock having half the frequency of said first clock, for generating first test data,

a second test pattern generation section, operating on said second clock, for generating second test data, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on the signal value of said second clock, thereby inputting the selected test data to said memory as third test data.

3. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a test pattern generation section, operating on a second clock having half the frequency of said first clock, for generating first test data,

an LSB0 processing section for generating second test data by adding numeric value 0 to said first test data generated by said test pattern generation section as the least significant bit thereof,

an LSB1 processing section for generating third test data by adding numeric value 1 to said first test data generated by said test pattern generation section as the least significant bit thereof, and

a test data selection section for selectively outputting either said second or third test data being output from said LSB0 processing section or said LSB1 processing section, respectively, depending on the signal

value of said second clock, thereby inputting the selected test data to said memory as fourth test data.

4. A semiconductor integrated circuit in accordance with claim 3, wherein a delay circuit for generating a delay clock obtained by delaying said second clock and for supplying said delay clock to said test data selection section is provided.

5. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a test pattern generation section, operating on a second clock having half the frequency of said first clock, for generating first test data,

an LSB0 processing section for generating second test data by adding numeric value 0 to said first test data generated by said test pattern generation section as the least significant bit thereof,

an LSB1 processing section for generating third test data by adding numeric value 1 to said first test data generated by said test pattern generation section as the least significant bit thereof,

a clock selection section capable of selecting either said second clock or the inverted clock of said second clock, and

a test data selection section for selectively outputting either said second or third test data being output from said LSB0 processing section or said LSB1 processing section, respectively, depending on the output of said clock selection section, thereby inputting the selected test data to said memory as fourth test data.

6. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a memory device for capturing first output data being output from said memory in synchronization with said first clock, depending on a second clock having half the frequency of said first clock, and

an expected value comparison section, operating on said second clock, for respectively comparing second output data being output from said memory device and third output data being output from said memory immediately after the output of said first output data with a predetermined expected value.

7. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a first test pattern generation section, operating on a second clock having the same frequency as that of said first clock, for generating first test data,

a second test pattern generation section, operating on a third clock, the inverted clock of said second clock, for generating second test data, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on either the signal value of said second clock or the signal value of said third clock, thereby inputting the selected test data to said double data rate memory as third test data.

8. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a first test pattern generation section, operating on a second clock having the same frequency of that of said first clock, for generating first test data,

a second test pattern generation section, operating on said second clock, for generating second test data, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on the signal value of said second clock, thereby inputting the selected test data to said double data rate

memory as third test data.

9. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a test pattern generation section, operating on a second clock having the same frequency as that of said first clock, for generating first test data,

an LSB0 processing section for generating second test data by adding numeric value 0 to said first test data generated by said test pattern generation section as the least significant bit thereof,

an LSB1 processing section for generating third test data by adding numeric value 1 to said first test data generated by said test pattern generation section as the least significant bit thereof, and

a test data selection section for selectively outputting either said second or third test data being output from said LSB0 processing section or said LSB1 processing section, respectively, depending on the signal value of said second clock, thereby inputting the selected test data to said double data rate memory as fourth test data.

10. A semiconductor integrated circuit in accordance with claim 9, wherein a delay circuit for generating a

delay clock obtained by delaying said second clock and for supplying said delay clock to said test data selection section is provided.

11. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a test pattern generation section, operating on a second clock having the same frequency as that of said first clock, for generating first test data,

an LSB0 processing section for generating second test data by adding numeric value 0 to said first test data generated by said test pattern generation section as the least significant bit thereof,

an LSB1 processing section for generating third test data by adding numeric value 1 to said first test data generated by said test pattern generation section as the least significant bit thereof,

a clock selection section capable of selecting either said second clock or the inverted clock of said second clock, and

a test data selection section for selectively outputting either said second or third test data being output from said LSB0 processing section or said LSB1 processing section, respectively, depending on the output of said clock selection section, thereby inputting the

selected test data to said double data rate memory as fourth test data.

12. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a memory device for capturing first output data being output from said double data rate memory in synchronization with said first clock, depending on a second clock having the same frequency as that of said first clock, and

an expected value comparison section, operating on said second clock, for respectively comparing second output data being output from said memory device and third output data being output from said double data rate memory immediately after the output of said first output data with a predetermined expected value.

13. A method of testing a memory operating on a first clock, comprising the steps of generating first test data depending on a second clock having half the frequency of said first clock, generating second test data depending on a third clock, the inverted clock of said second clock, selecting either said first or second test data depending on either the signal value of said second clock or the signal value of said third clock, and inputting the selected test data to said memory as third test data.

14. A method of testing a memory operating on a first clock, comprising the steps of generating first test data depending on a second clock having half the frequency of said first clock, generating second test data by adding numeric value 0 to said first test data as the least significant bit thereof, generating third test data by adding numeric value 1 to said first test data as the least significant bit thereof, selecting either said second or third test data depending on the signal value of said second clock, and inputting the selected test data to said memory.

15. A method of testing a memory operating on a first clock, comprising the steps of holding first data being output from said memory in synchronization with said first clock as second data depending on a second clock having half the frequency of said first clock, and respectively comparing said second data and third data being output in synchronization with said first clock from said memory immediately after the output of said first data with a predetermined expected value depending on said second clock.

16. A method of testing a double data rate memory operating on a first clock, comprising the steps of

generating first test data depending on a second clock having the same frequency as that of said first clock, generating second test data depending on a third clock, the inverted clock of said second clock, selecting either said first or second test data depending on either the signal value of said second clock or the signal value of said third clock, and inputting the selected test data to said double data rate memory as third test data.

17. A method of testing a double data rate memory operating on a first clock, comprising the steps of generating first test data depending on a second clock having the same frequency as that of said first clock, generating second test data by adding numeric value 0 to said first test data as the least significant bit thereof, generating third test data by adding numeric value 1 to said first test data as the least significant bit thereof, selecting either said second or third test data depending on the signal value of said second clock, and inputting the selected test data to said double data rate memory.

18. A method of testing a double data rate memory operating on a first clock, comprising the steps of holding first data being output from said double data rate memory in synchronization with said first clock as second data

depending on a second clock having th same frequency as that of said first clock, and respectively comparing said second data and third data being output in synchronization with said first clock from said double data rate memory immediately after the output of said first data with a predetermined expected value depending on said second clock.

19. A semiconductor integrated circuit in accordance with claim 1, wherein a delay circuit for generating a delay clock obtained by delaying said second clock and for supplying said delay clock to said test data selection section is provided.

20. A semiconductor integrated circuit in accordance with claim 2, wherein a delay circuit for generating a delay clock obtained by delaying said second clock and for supplying said delay clock to said test data selection section is provided.

21. A semiconductor integrated circuit in accordance with claim 7, wherein a delay circuit for generating a delay clock obtained by delaying said second clock and for supplying said delay clock to said test data selection section is provided.

22. A semiconductor integrated circuit in accordance with claim 8, wherein a delay circuit for generating a delay clock obtained by delaying said second clock and for supplying said delay clock to said test data selection section is provided.

23. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a first test pattern generation section, operating on a second clock having half the frequency of said first clock, for generating first test data,

a second test pattern generation section, operating on a third clock, the inverted clock of said second clock, for generating second test data,

a clock selection section capable of selecting either said second clock or the inverted clock of said second clock, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on the output of said clock selection section, thereby inputting the selected test data to said memory as third test data.

24. A semiconductor integrated circuit comprising:

a memory operating on a first clock,

a first test pattern generation section, operating on a second clock having half the frequency of said first clock, for generating first test data,

a second test pattern generation section, operating on said second clock, for generating second test data,

a clock selection section capable of selecting either said second clock or the inverted clock of said second clock, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on the output of said clock selection section, thereby inputting the selected test data to said memory as third test data.

25. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a first test pattern generation section, operating on a second clock having the same frequency as that of said first clock, for generating first test data,

a second test pattern generation section, operating on a third clock, the inverted clock of said second clock,

for generating second test data,

a clock selection section capable of selecting either said second clock or the inverted clock of said second clock, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or said second test pattern generation section, respectively, depending on the output of said clock selection section, thereby inputting the selected test data to said double data rate memory as third test data.

26. A semiconductor integrated circuit comprising:

a double data rate memory operating on a first clock,

a first test pattern generation section, operating on a second clock having the same frequency as that of said first clock, for generating first test data,

a second test pattern generation section, operating on said second clock, for generating second test data,

a clock selection section capable of selecting either said second clock or the inverted clock of said second clock, and

a test data selection section for selectively outputting either said first or second test data being output from said first test pattern generation section or

said second test pattern generation section, respectively, depending on the output of said clock selection section, thereby inputting the selected test data to said double data rate memory as third test data.